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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kie Y. Ahn et al.

Title: BIPOLAR TRANSISTORS WITH LOW-RESISTANCE EMITTER CONTACTS

Docket No.: 303.466US1
Filed: April 29, 1998
Examiner: W. David Coleman

Serial No.: 09/069,668
Due Date: October 21, 2000
Group Art Unit: 2823

Box AF
Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

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X A Response (3 Pages).
X Petition for Extension of Time (1 pg.)
X A check in the amount of $110.00 to cover the Extension of Time Fee.

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

By: _____
Atty. Eduardo E. Drake
Reg. No. 40,594

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EXPEDITED PROCEDURE - EXAMINING GROUP 2823

S/N 09/069,668 PATENT

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#10 10-29-00

RESPONSE UNDER 37 C.F.R. § 1.116

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REMARKS

This response addresses the Final Office Action mailed on June 21, 2000. Claims 1-30 and 32-39 are pending in this application. Of these, claims 29 and 30 have been allowed.

Applicant reserves the right to address any of the Examiner's tacit or explicit characterizations of the references to the extent the following remarks do not.

Response to §102 Rejections

The Examiner rejected claims 1-5, 7-28, and 32-39 under 35 U.S.C.§102(b) as anticipated by Takemura (U.S. Patent 5,587,326). However, applicant respectfully submits that Takemura fails to meet all the requirements of these claims.

For example, claim 1 requires "substituting metal for at least a portion of the polysilicon structure to produce a metal emitter contact entirely above the surface of the substrate at the emitter region position." In contrast, Takemura fails to make any form of substitution of metal for polysilicon. Instead, Takemura reports formation of a stack of polysilicon layer 23 and conductive film 22 over base region 19. After formation of the stack, Takemura reports implanting arsenic ions by ion implantation into polysilicon layer 23 and then use of thermal diffusion to drive the arsenic ions through the conductive film into the base region, forming emitter region 24. Takemura further reports forming electrodes 25a, 25b, and 25c after forming the emitter region. See column 4, lines 66 - column 5, line 17.

The Examiner contends that Takemura shows that "aluminum layer 25a is substituted for a portion of the emitter contact region to completely fill the hole." No textual support is cited for this contention, and indeed, there appears to be none for it. Accordingly, applicant respectfully requests reconsideration and withdrawal of the rejection of claim 1 and its dependents.

With the exception of claim 18 and its dependents, all the other rejected claims requires at least some substitution of metal for polysilicon. Accordingly, applicant respectfully requests reconsideration and withdrawal of the rejection of these claims.

Claim 18 requires "heating at least the deposited metal and the polysilicon structure to urge diffusion of the deposited metal into the polysilicon layer, with the doped diffusion barrier layer inhibiting diffusion of the deposited metal into the emitter region position of the transistor." Takemura, in contrast, reports use of thermal diffusion to drive arsenic ions implanted in its polysilicon layer through conductive film 22 into the base region to form emitter region 24, and then formation of electrodes 25a, 25b, and 25c atop the polysilicon layer. Thus, conductive film does not appear to be a diffusion barrier . Accordingly, the rejection of claim 18 and its dependents should also be withdrawn.

CONCLUSION

In view of the foregoing remarks, applicant respectfully requests reconsideration and withdrawal of the rejections. Moreover, applicant invites the Examiner to telephone its patent counsel Eduardo Drake at (612) 349-9593 to resolve or discuss any issues which may impede allowance of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

KIE Y. AHN ET AL.

By their Representatives,

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Date 23 Oct. 2000 By _____
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Box AF, Commissioner of Patents, Washington, D.C. 20231 on **October 23, 2000.**

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